CLAIMS

Having thus described our invention, what we claim as new and desire to secure by Letters Patent is as follows:

1. A method of forming a semiconductor substrate, comprising:

forming a metal back-gate over a substrate;

forming a passivation layer on the metal back-gate to prevent the metal back-gate from reacting with radical species; and

providing an intermediate gluing layer on said passivation layer to enhance adhesion between said metal back-gate and said substrate.

2. The method of claim 1, wherein said intermediate layer comprises one of a-Si, Si_3N_4 and a combined layer of a-Si and Si_3N_4 .

3. The method of claim 1, wherein said forming of said metal back-gate includes depositing W, and

said forming of said passivation layer is performed after said W deposition, said passivation layer being a thin W passivation layer.

4. The method of claim 3, wherein said depositing of said W comprises a plasma vapor deposition (PVD) of W.

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5. The method of claim 3, wherein said depositing of said W comprises a chemical vapor deposition (CVD) of W.

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6. The method of claim 1, wherein said forming of said metal back-gate comprises:

conducting UHV desorption of native oxide on W under a pressure of 10^{-9} torr at 750°C for 5 minutes;

forming a monolayer of W-Si silicide at 625°C for 1.5 min. reaction with SiH_4 such that a bare W surface reacts with Si to form a monolayer of W-Si; and

performing nitridation of W-Si at 750°C for 30 min. with NH_3 and reacting active NH_2 with W-Si to form W-Si-N.

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7. The method of claim 1, wherein said metal back-gate is formed of a metal having a high melting temperature to withstand thermal treatment during semiconductor processing.

8. The method of claim 7, wherein said metal back-gate comprises one of tungsten and titanium nitride.

9. The method of claim 1, wherein said substrate comprises a silicon-on-insulator substrate having a gate oxide formed thereon.

10. The method of claim 9, wherein said metal back-gate comprises a tungsten layer, said tungsten layer being deposited on the gate oxide.

11. The method of claim 1, wherein the metal back-gate comprises a W layer, and wherein a low temperature oxide (LTO) is deposited on the W layer.

12. The method of claim 1, wherein said substrate with a multilayer stack is bonded to a silicon substrate and annealed to strengthen the bond across the bonding interface.

13. The method of claim 11, wherein said W layer is passivated before the LTO deposition to prevent the reaction of tungsten with oxygen and the delamination at the W-SiO_2 interface.

14. The method of claim 1, further comprising annealing said metal back-gate and said substrate.

15. The method of claim 14, wherein said annealing occurs at temperatures below 1100 °C.

16. The method of claim 15, wherein annealing conditions including any of a ramp-up rate, a ramp-down rate, a stablization temperature, and a stabilization temperature time are optimized to minimize stress induced by thermal mismatch of different materials of said metal back-gate, said substrate, said passivation layer and said intermediate gluing layer.

17. The method of claim 1, wherein said intermediate layer comprises a Si-based intermediate layer.

18. A method of forming a semiconductor substrate, comprising:

forming a metal back-gate over a substrate; and

providing a passivation layer between said substrate and said metal back-gate to enhance adhesion therebetween.

19. A method of forming a semiconductor substrate, comprising:

growing a gate oxide on a silicon-on-insulator (SOI) material;

depositing a refractory metal onto said gate oxide; and

forming a passivation layer on said refractory metal.

20. The method of claim 19, further comprising:

depositing an insulator on said metal to form a multi-layer stack;

bonding said multi-layer stack to a second substrate, to form a bonded structure; and

annealing said bonded structure.

21. The method according to claim 19, wherein said insulator comprises one of a low temperature oxide, SiN and AlOx.

22. A semiconductor device, comprising:

a substrate;

a metal back-gate formed over said substrate;

a passivation layer formed on the metal back-gate to prevent the metal from reacting with radical species; and

an intermediate gluing layer formed on said passivation layer to enhance adhesion between said metal back-gate and said substrate.

23. The device of claim 22, wherein said intermediate layer comprises one of a-Si, Si_3N_4 and a combined layer of a-Si and Si_3N_4 .

24. The device of claim 22, wherein said metal back-gate includes W, and said passivation layer comprises a thin W passivation layer.

25. The device of claim 23, wherein said W comprises a plasma vapor deposition (PVD) W.

26. The device of claim 23, wherein said W comprises a chemical vapor deposition (CVD) W.

27. The device of claim 22, wherein said metal back-gate comprises:

an UHV desorption of native oxide on W formed under a pressure of 10^{-9} torr at 750°C for 5 minutes;

a monolayer of W-Si silicide formed at 625°C for 1.5 min. reaction with SiH_4 such that a bare W surface reacts with Si to form a monolayer of W-Si; and

a nitridation of W-Si formed at 750°C for 30 min. with NH_3 and reacting active NH_2 with W-Si to form W-Si-N.

28. The device of claim 22, wherein said metal back-gate is formed of a metal having a high melting temperature to withstand thermal treatment during semiconductor processing.

29. The device of claim 22, wherein said metal back-gate comprises one of tungsten and titanium nitride.

30. The device of claim 22, wherein said substrate comprises a silicon-on-insulator substrate having a gate oxide formed thereon.

31. The device of claim 22, wherein said metal back-gate comprises a tungsten layer, said tungsten layer being deposited on the gate oxide.

32. The device of claim 22, wherein the metal back-gate comprises a W layer, and wherein a low temperature oxide (LTO) is deposited on the W layer.

33. The device of claim 22, wherein said substrate with a multilayer stack is bonded to a silicon substrate and annealed to strengthen the bond across the bonding interface.

34. The device of claim 32, wherein said W layer is passivated before the LTO deposition to prevent the reaction of tungsten with oxygen and the delamination at the W-SiO_2 interface.

35. The device of claim 22, wherein said intermediate layer comprises a-Si-based intermediate layer.

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